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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,064	12/09/2003	Zvi Or-Bach	38897-199163	2943

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EXAMINER	
QUACH, TUAN N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,064	OR-BACH ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The abstract of the disclosure is objected to because it appears to correspond to the non-elected invention of claim 2, namely the method of fabricating the semiconductor device as opposed to the semiconductor device in claims 1 and 3-18. Correction is required. See MPEP § 608.01(b).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3-5, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al.

Regarding claims 1 and 18, Shenoy 5,994,766 teaches the logic array comprising repeating core and at least one of area of I/Os being configurable, e.g., Fig.

1, column 4 line 66 to column 5 line 11 wherein the I/0 slots are arranged in linear arrays of cells or titles and wherein the repeating core correspond to the one or more logic circuit and associated I/0. Shenoy lacks primarily the recitation of the borderless array and the same metal in all the configuration.

Sivilotti et al., 6,316,334 B1 teaches the use of borderless arrays which can be cut to prevent substantial waste. See column 1 line 50 to column 2 line 24.

It would have been obvious to one skilled in the art in practicing the Shenoy invention to have employed borderless array since such is conventional and advantageous to prevent substantial waste as suggested by Sivilotti et al. The use of a at least one metal which is the same for all I/O configuration would have been obvious corresponding to the processing step as opposed to a structural difference; the use of the same metal layer would have been further obvious and advantageous wherein the same metal layer can be patterned in the same step or using the same masking, as opposed to using different metal layer for different I/O. Such would have been further obvious as evident in Sivilotti et al., column 3 lines 53-62.

Regarding claims 3 and 16-17, Shenoy teaches a semiconductor device comprising a logic array 19/100, areas I/Os 26, redistribution layer 108 for redistributing at least some of said area I/Os. See column 4, line 1 to column 8, line 20. The configurable I/O in claim 17 is discussed as above regarding claims 1 and 18. Although Shenoy does not recite the borderless array, such would have been conventional and obvious as evidenced by Sivilotti et al. as delineated above. The arrangement of I/O cells in desired patterns and suitable spacing as in claims 4 and 5 is

well within the purview of one skilled in the art and as evidenced by Shenoy above, and as such would have been obvious.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al. as applied to claims 1, 3-5, 16-18 above, and further in view of the IBM TDB publication 6/86, Vol. 29, No. 1, pp. 88-94 (Multi-function FET I/O Masterslice cell) and Cox.

Regarding claims 6-8, the use of at least two metal layers for the repeating pattern would have been obvious since Shenoy further shows at least one pad 52 used to connect the semiconductor device to other devices overlays at least a portion of the logic array or a portion of area I/Os, column 7, lines 64-66 and as evidenced by the IBMTDB article, Fig. 3, and the associated disclosure wherein at least one metal layer M(1), and including two metal layers M(1) and M(2) can be employed for all I/O configurations. Such would have been further obvious as evidenced by Cox 6,693,454 which teaches customization using via layer masks wherein at least some of the plurality of the metal layers are customized and used to configure the device for specific application, thereby permitting the same metal layers being employed. See column 2 lines 2-41, line 60 to column 6 line 56, particularly column 6 lines 28-36, lines 50-56.

Claims 9-10, 11-12 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al. and the IBM TDB article or Cox as applied to claims 6-8 above and further in view of Hively.

The references are applied as above including the repeating I/O cells in claims 11 and 12 are delineated above, including in Shenoy and as evidenced in Sivilotti et al.,

Fig. 3, 8, column 3 line 2 to column 4 line 3. The references as applied above do not recite the customized layers as in claims 9-12 and/or connections using customized via layers as in claims 13-15.

Additionally, Hively et al. (5,514,884) teaches the provision of customized layers to achieve advantages including avoidance of blocks of circuitry, defective control logic, defective bus line, and to select the organization of the final structure. See column 3 lines 25 to column 4 line 50, particularly column 3 lines 51 to column 4 line 11.

Cox 6,693,454 is applied as above and teaches customization using via layer masks wherein at least some of the plurality of the metal layers are customized and used to configure the device for specific application. See column 2 lines 2-41, line 60 to column 6 line 56, particularly column 6 lines 28-36, lines 50-56.

It would have been obvious to one skilled in the art to have employed in the invention above to have employing additional custom layers since such is conventional and advantageous as evidenced by Hively et al. or Cox to obtain the desired applications.

Regarding claims 13-15, the I/O cells comprising at least two electronic components and multiple possible connections therebetween would have been obvious and conventional as shown in Shenoy, Fig. 1, column 4 line 66 to column 5 line 11 wherein the electronic components and interconnections therein are taught, e.g., column 5 line 11, and additionally, such multiple components and connections therebetween would have been conventional and obvious as taught by Hively et al., portions delineated above, including column 4 lines 4 lines 11-50, the abstract, wherein

the desired electrical connections can be made by the customized via layers after all active and conductive layers have been manufactured. The connections using customized via layers would have been further conventional and obvious as taught by Cox, wherein electrical components and desired connections therebetween are also shown, see e.g., the portions delineated above, column 2 lines 2-40 wherein the use of custom via layer for connections would have been apparent, e.g., column 2 lines 20-26.

Applicant's arguments filed June 10, 2005 have been fully considered but they are not persuasive.

Initially, the Terminal Disclaimer filed June 10, 2005 has been accepted and the double patenting rejection has been withdrawn.

Applicant argues that configurable I/O are not taught by Shenoy or Sivilotti et al. These references nonetheless does not preclude such configurable I/O; applicant has not pointed out patentable difference between the respective I/O. The intended use of such I/O to be configured would not distinguish the claimed features from the prior art – if the prior art has the capability so perform. See MPEP 2114 and *Ex parte Marsham,* 2 USPQ2d 1647 (1987). The recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber*, 44 USPQ2d 1429 (Fed. Cir. 1997). To the extent that such I/O would require the customized via layers to provide the configuration, such use of customized via layers would have been further conventional and obvious as amply evidenced by Hively et al. and Cox as applied above, evidencing the conventionality and advantages of customization to configure the device for specific applications.

Applicant further argues that the prior art does not show a repeating module. Nonetheless, this does not take into account the logic cells and I/O cells shown in Shenoy, e.g., the portions delineated above, including column 4 line 66 to column 5 line 5. See additionally the teachings in Sivilotti above, particularly column 1 line 66 to column 2 line 14 wherein the repetition of arrays is readily apparent on the wafer of a bordeless array which compsed of micro arrays or blocks including portions thereof for input/output connections.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach
Primary Examiner